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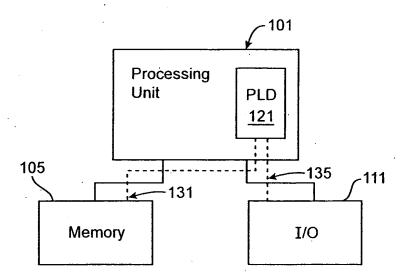


FIG. 1

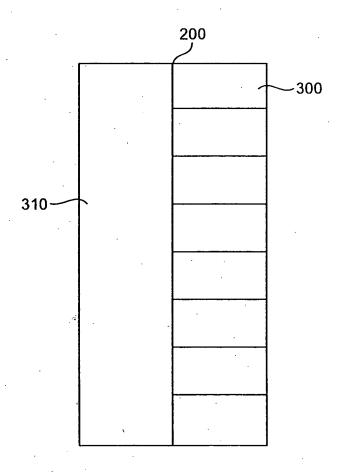
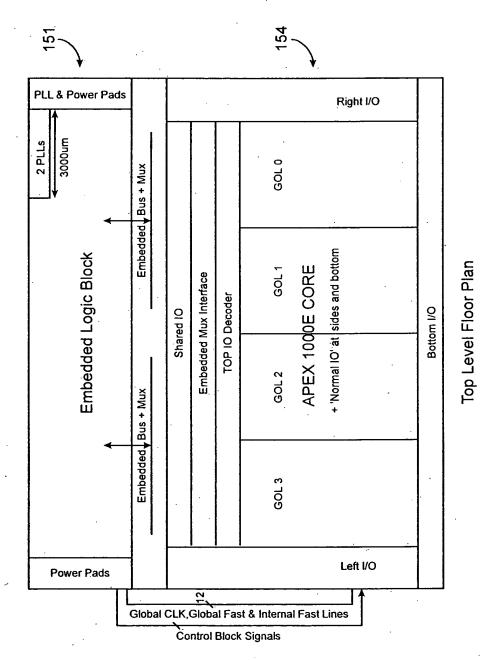


FIG. 4



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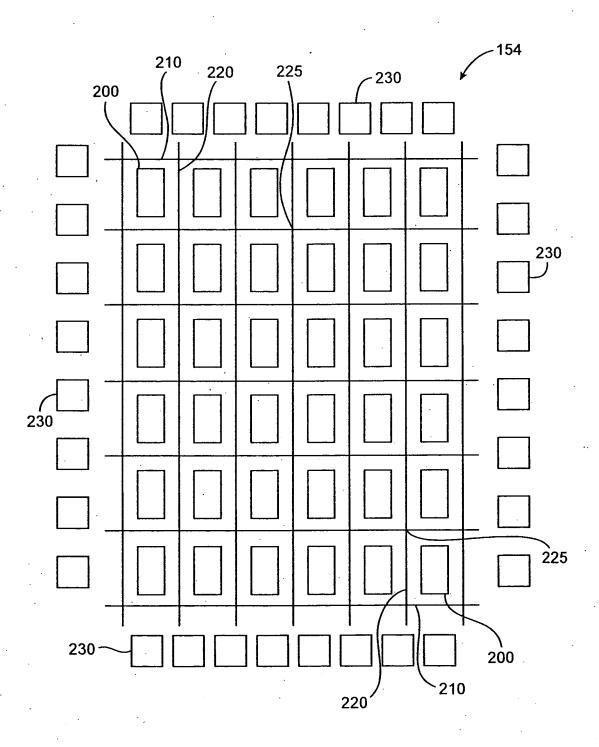
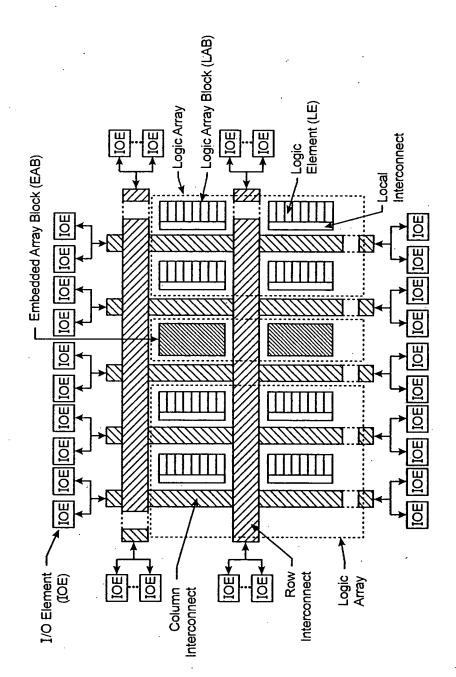


FIG. 3



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<u>G.</u> 5



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To/From Adjacent LAB, ESB, or IOEs two local interconnect areas. These LEs can drive two local interconnect areas. The 10 LEs in the LAB are driven by GHJ Local Interconnect To/From Adjacent LAB, ≼ ESB, or IOEs LEs drive local, MegaLAB, row, \_ and column interconnects MegaLAB Interconnect

FIG. 6



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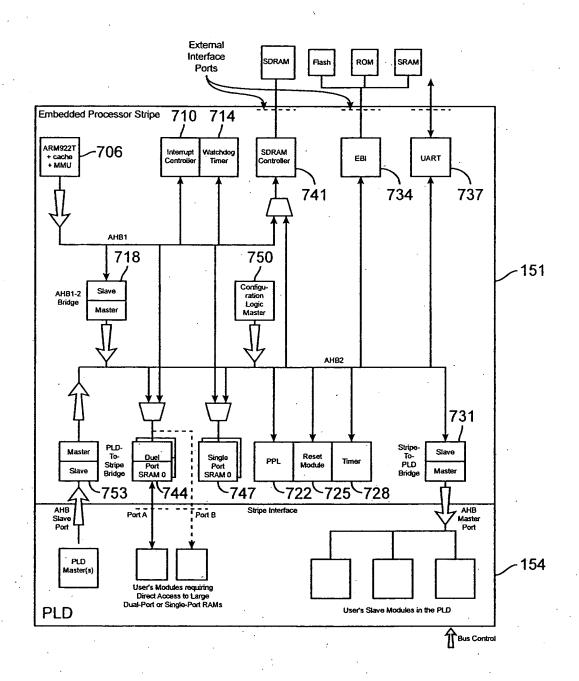


FIG. 7



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FIG. 8

Programmable Logic

FIG. 9

Embedded Processor Stripe

FIG. 10

Stretched
Portion

Programmable
Logic

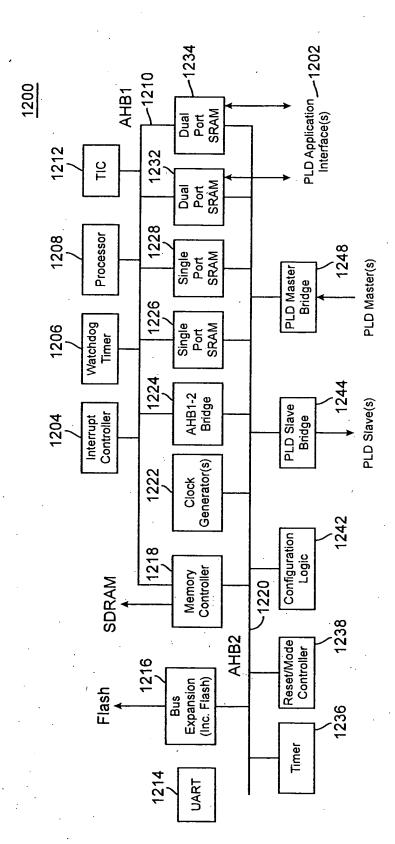
Embedded Processor Stripe

FIG. 11

Embedded
Processor Stripe
Programmable
Logic



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-1G. 12

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32				
8K	<b>↑</b> 4K <b>↓</b>			
	<b>←</b> .8 →			

FIG. 13A

8K X 32

16 ↑ 4K ← 8 → ↓

FIG. 13B

16K X 16

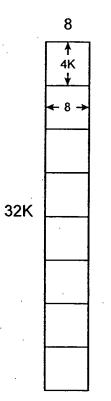
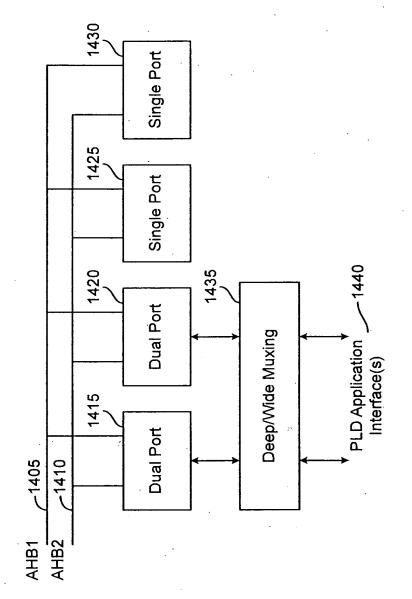


FIG. 13C

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<u>1500</u>

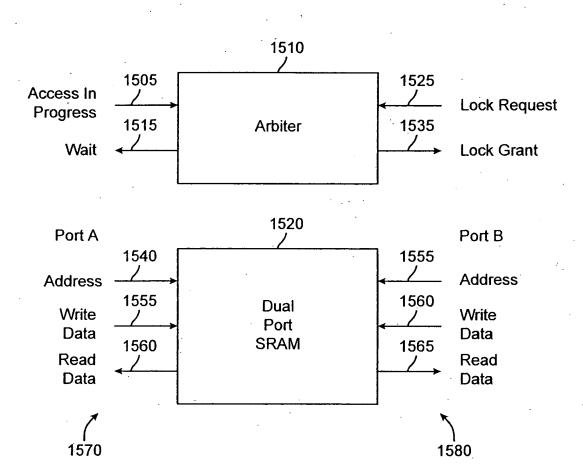


FIG. 15



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1600

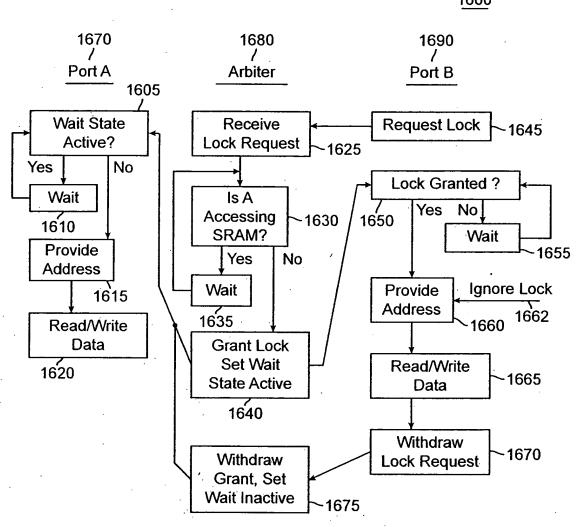


FIG. 16



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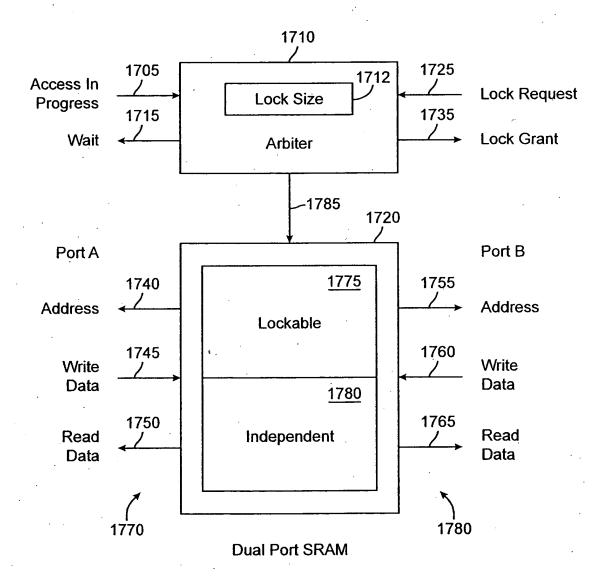


FIG. 17



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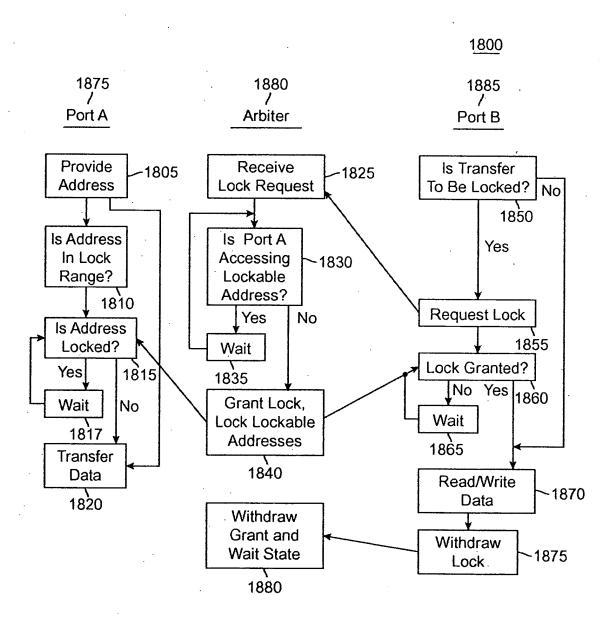
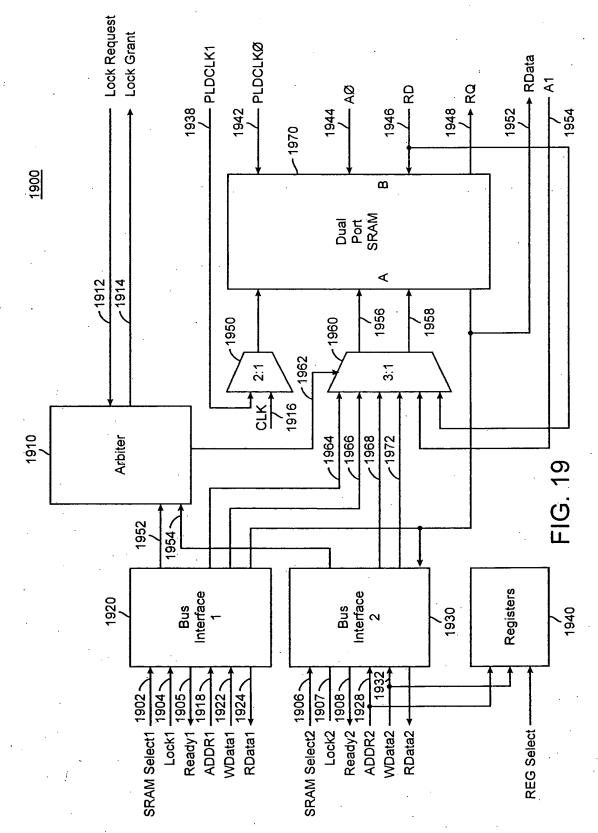


FIG. 18

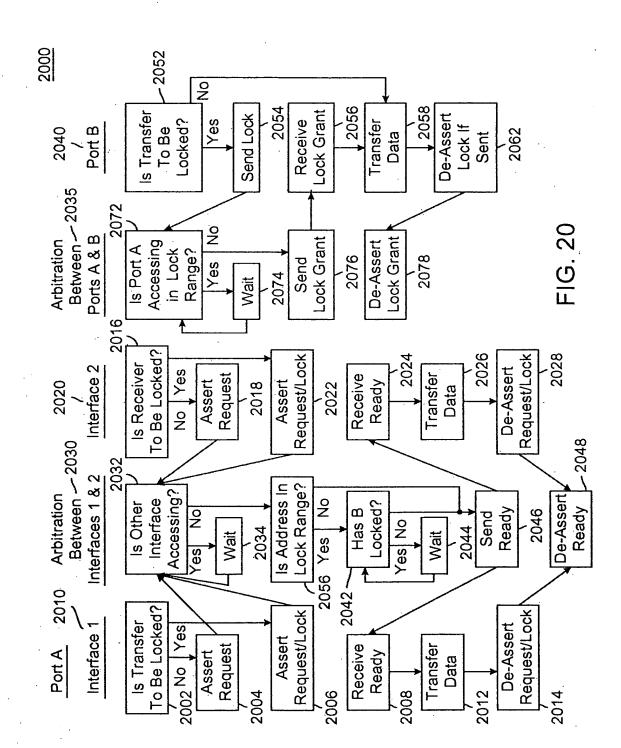


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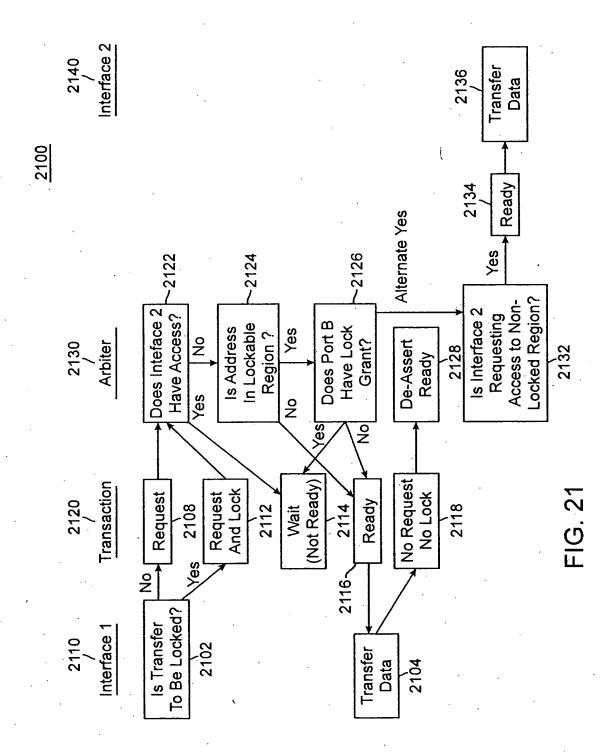
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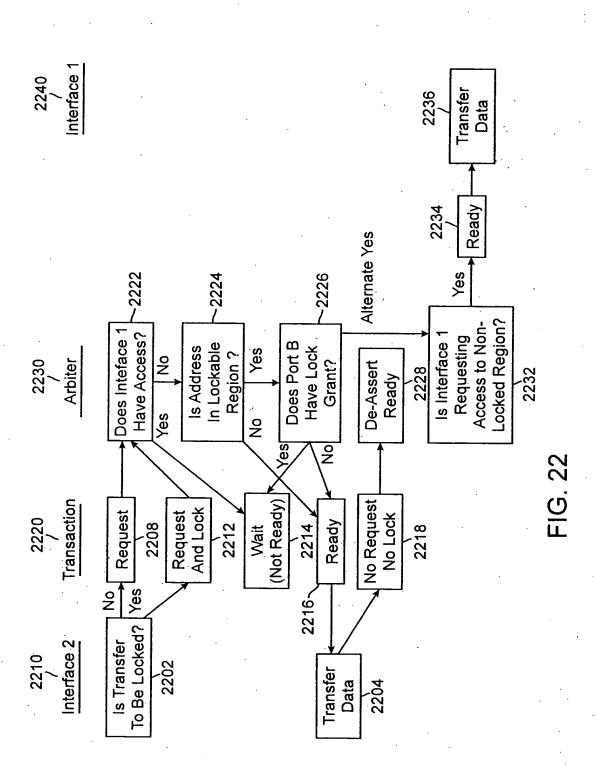
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## 2300

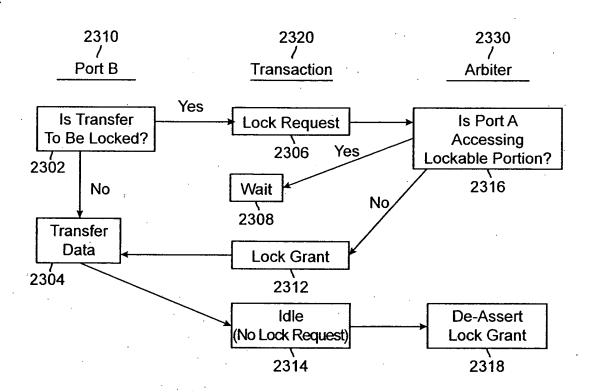


FIG. 23



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2400 2410 2420 Port A Port B Interface 1 Interface 2 PLP Interface **Needs Access** 2430 **Needs Access Needs Access** 2455 2405 Is Interface 2 Is Interface 1 Locked 2435 -Accessing? Accessing? 2460 Transfer? No 2415 Yes No No Yes Yes Compare Address Wait 2440 To Lock Range 2425 Is Port A Accessing In 2465 Lock Range? Address in Lock Range? 2445 No Yes Wait Interface Has Port B 2470 2450° **May Access Been Granted** No 2485 Lock? Yes Wait (Or Let Other 2490 Interface Access)

FIG. 24



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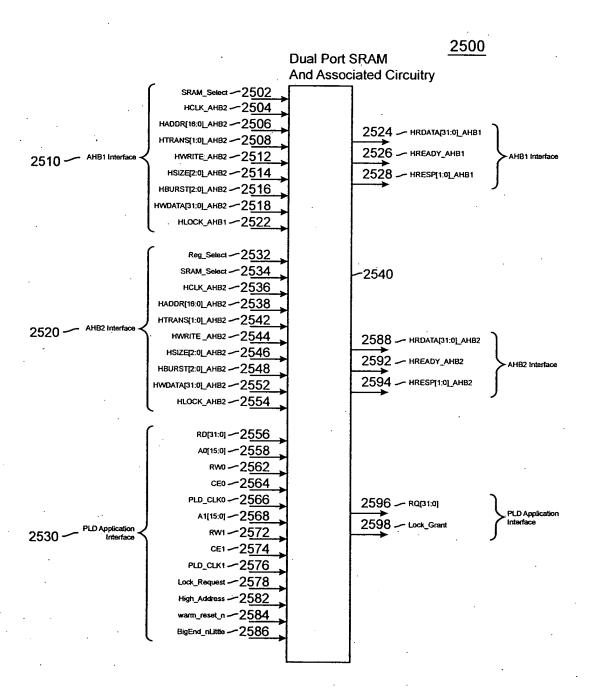


FIG. 25